ABSTRACT OF THE DISCLOSURE

An integrated memory has a memory cell array having word lines and bit lines. The bit lines are organized in bit line pairs. The bit lines of the bit line pairs cross one another at a crossing location and run parallel to one another. A sense amplifier is connected to one of the bit line pairs at one end. Two precharge circuits are provided. One precharge circuit is arranged on a side of the crossing location and the other precharge circuit is arranged on a side of the crossing location. The precharge circuit facing the sense amplifier is arranged at a first distance from the crossing location and at a second distance from the sense amplifier. The RC constant of the bit lines, which is effective during the precharge operation, is reduced, so that the time period required for a precharge operation is reduced.